Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 9, with the following rewritten paragraph:

This application relates to the following commonly assigned co-pending applications entitled:

~~"Seen Wheel An Apparatus~~ And Method For Interfacing A High Speed Scan-Path With A ~~Slow~~ Speed Tester Equipment," Serial No. 09/653,642 (now US Patent No 6,779,142), filed August 31, 2000, ~~Attorney Docket No. 1662-23700~~; "Priority ~~Rotary~~ Rules For Reducing Network Message Routing Latency ~~And Coherence Dependence Priority Rule~~," Serial No. 09/652,322 (now US Patent No 6,961,781), filed August 31, 2000, ~~Attorney Docket No. 1662-27300~~; "~~Speculative~~ Scalable Directory Based Cache Coherence Protocol," Serial No. 09/652,703 (now US Patent No 6,633,960), filed August 31, 2000, ~~Attorney Docket No. 1662-27400~~; "Scalable Efficient I/O Port Protocol," Serial No. 09/651,391 (09/652591, now US Patent No 6,738,836), filed August 31, 2000, ~~Attorney Docket No. 1662-27500~~; "Efficient Translation Lookaside Buffer Miss Processing In Computer Systems ~~For Applications Using Large Pages In Systems~~ With A Large Range Of Page Sizes ~~By Eliminating Page Table Level~~," Serial No. 09/652,552 (now US Patent No 6,715,057), filed August 31, 2000, ~~Attorney Docket No. 1662-27600~~; "Fault Containment And Error Recovery Techniques In A Scalable Multiprocessor," Serial No. 09/651,949 (now US Patent No 6,678,840), filed August 31, 2000, ~~Attorney Docket No. 1662-27700~~; "Speculative Directory Writes In A Directory Based Cache Coherent ~~CC~~ Non-Uniform Memory Access Protocol," Serial No. 09/652,834 (now US Patent No 7,099,913), filed August 31, 2000, ~~Attorney Docket No. 1662-27800~~; "Special Encoding Of Known Bad Data," Serial No. 09/652,314 (now US Patent No 6,662,319), filed August 31, 2000, ~~Attorney Docket No. 1662-27900~~; "Broadcast Invalidate Scheme," Serial No. 09/652,165 (now US Patent No 6,751,721), filed August 31, 2000, ~~Attorney Docket No. 1662-28000~~; "Mechanism To Track ~~Keep~~ All Open Pages ~~Open~~ In A DRAM Memory System," Serial No. 09/652,704 (now US Patent No 6,662,265), filed August 31, 2000, ~~Attorney Docket No. 1662-28100~~; "Programmable DRAM Address Mapping Mechanism," Serial No. 09/653,093 (now US Patent No 6,546,453), filed August 31, 2000, ~~Attorney Docket No. 1662-28200~~; "Computer Architecture And System For Efficient

~~Management Mechanism To Enforce Memory Read/Write Fairness, Avoid Tristate Bus Conflicts, And Maximize Memory Bandwidth~~," Serial No. 09/652,323, filed August 31, 2000, ~~Attorney Docket No. 1662-29200~~; "An Efficient Address Interleaving With Simultaneous Multiple Locality Options," Serial No. 09/652,452, filed August 31, 2000, ~~Attorney Docket No. 1662-29300~~; "A High Performance Way Allocation Strategy For A Multi-Way Associative Cache System," Serial No. 09/653,092, filed August 31, 2000, ~~Attorney Docket No. 1662-29400~~; "Method And System For Absorbing Defects In High Performance Microprocessor With A Large N-Way Set Associative Cache," Serial No. 09/651,948, filed August 31, 2000, ~~Attorney Docket No. 1662-29500~~; "A Method For Reducing Directory Writes And Latency In A High Performance, Directory-Based, Coherency Protocol," Serial No. 09/652,324, filed August 31, 2000, ~~Attorney Docket No. 1662-29600~~; "Mechanism To Reorder Memory Read And Write Transactions For Reduced Latency And Increased Bandwidth," Serial No. 09/653,094, filed August 31, 2000, ~~Attorney Docket No. 1662-30800~~; "~~Look Ahead Mechanism To~~ System For Minimizing ~~Memory~~ And ~~Manage~~ Bank Conflicts In A Computer ~~Memory~~ System," Serial No. 09/652,325, filed August 31, 2000, ~~Attorney Docket No. 1662-30900~~; "Computer Resource Management And Allocation System~~Scheme That Ensures Forward Progress, Maximizes Utilization Of Available Buffers And Guarantees Minimum Request Rate~~," Serial No. 09/651,945, filed August 31, 2000, ~~Attorney Docket No. 1662-31000~~; "~~Input Data Recovery Scheme~~," Serial No. 09/653,643, filed August 31, 2000, ~~Attorney Docket No. 1662-31100~~; "Fast Lane Prefetching," Serial No. 09/652,451, filed August 31, 2000, ~~Attorney Docket No. 1662-31200~~; "Mechanism For Synchronizing Multiple Skewed Source-Synchronous Data Channels With Automatic Initialization Feature," Serial No. 09/652,480, filed August 31, 2000, ~~Attorney Docket No. 1662-31300~~; and "Chaining Directory Reads And Writes To Reduce DRAM Bandwidth In A Directory Based CC-NUMA Protocol," Serial No. 09/652,315, filed

now US Patent No 6,904,817
now US Patent No 6,557,900
now abandoned
now US Patent No 6,671,822
now US Patent No 6,654,858
now US Patent No 6,591,349
now US Patent No 6,622,225
now US Patent No 6,754,739
now US Patent No 6,668,335
now US Patent No 6,681,295
now US Patent No 6,636,955

"System for recovery of data in a multi-processor system comprising a conduction path for each bit between processors where the paths are grouped into separate bundles and routed along different path"

now US Patent No 6,546,465

August 31, 2000~~, Attorney Docket No. 1662-31500~~, all of which are incorporated by reference herein.